Department of Electrical and Computer Engineering
The Johns Hopkins University
520.137 Introduction to Electrical and Computer Engineering – Fall 2018

Homework Assignment V

Reading Assignment: Kuc Chapter 4 and Kerns-Irwin Chapter 13

1. You need a few inverters in your circuit design. Unfortunately, the stock room only carries NAND and/or NOR gates.

   (a) Can you design INVERTERS from NAND gates? Please elaborate. Sketch your design if the answer is YES.

   (b) Can you design INVERTERS from NOR gates? Please elaborate. Again, sketch your design if the answer is YES.

2. Consider the design of a digital divisible-by-3 circuit which takes in as inputs a 4-bit non-negative binary number $X_3X_2X_1X_0$ and outputs a **1** whenever the decimal equivalence of the binary input is divisible by the decimal number 3. In other words, the circuit yields a **0** output when the input in decimal is not a multiple of 3. Note that zero is considered to be divisible by 3.

   (a) Construct the truth table for the 4-input (X_3 X_2 X_1 X_0) divisible-by-3 circuit.

   (b) Find the simplified Boolean expression for the output Y in terms of the inputs $\{X_3, X_2, X_1, X_0\}$.

   (c) Implement the divisible-by-3 circuit using only basic gates: INVERTER, 2-input AND, 2-input OR, and 2-input XOR gates.

   (d) What about a divisible-by-2 circuit (in other words, an even-number detection circuit)?

   (e) Design a divisible-by-6 circuit. Implement your modified design with basic gates. Can you take advantage of what you already have?

3. Consider the design of a multiplier which accepts two 3-bit non-negative binary numbers – $A_2A_1A_0$ and $B_2B_1B_0$ – as inputs and yields the 6-bit output $Y_5Y_4Y_3Y_2Y_1Y_0$. Assume that the stock room has an ample supply of basic gates as well as full adders.

   (a) Why do we need 6 bits to represent the multiplication output?

   (b) Find the logic function for Y_0, the least significant bit (LSB) of the output.

   (c) Find the logic function for Y_1, the next to least significant bit (LSB) of the output.

   (d) Sketch your implementation of the multiplier.
   Hint: compute the partial products, then use a cascade of full adders (beware of the shift) to sum up the final result.

Due date: **Friday October 19** in class